Jc997 U.S. PTO
10/024661
12/13/01

708

N

U.S. **UTILITY** Patent Application

P

PATENT NUMBER and ISSUE DATE

APPL NUM	FILING DATE	CLASS	SUBCLASS	GAU	EXAMINER
10024661	12/13/2001	326		2819	

**APPLICANTS: El-Ayat Khaled;

**CONTINUING DATA VERIFIED:
THIS APPLICATION IS A CON OF 09/738,508 12/18/2000
WHICH IS A DIV OF 09/224,929 12/31/1998 PAT 6,242,943

BEST AVAILABLE COPY

** FOREIGN APPLICATIONS VERIFIED:

PG-PUB	DO NOT PUBLISH ☒	RESCIND ☐	
Foreign priority claimed	☐ yes ☐ no	ATTORNEY DOCKET NO	
35 USC 119 conditions met	☐ yes ☐ no	ACT-320 COA	
Verified and Acknowledged Examiner's initials			

TITLE : Programmable multi-standard I/O architecture for FPGAs

U.S.DEPT. OF COMM./PAT & TM-PTO-435L(Rev. 12-94)

NOTICE OF ALLOWANCE MAILED	Assistant Examiner	CLAIMS ALLOWED	
		Total Claims	Print Claim for O.G

ISSUE FEE		DRAWING		
Amount Due	Date Paid	Sheets Drwg.	Figs.Drwg.	Print Fig.

☐ TERMINAL DISCLAMER	Primary Examiner	Application Examiner
	PREPARED FOR ISSUE	

WARNING: The information disclosed herein may be restricted. Unauthorized disclosure may be prohibited by the United States Code Title 35, Sections 122, 181 and 368, Possession outside the U.S. Patent & Trademark Office is restricted to authorized employees and contractors only.

FILED WITH: ☐ DISK (CRF) ☐ CD-ROM
(Attached in pocket on right inside flap)